## Remarks

The present amendment responds to the final Official Action dated September 15, 2004. The final Official Action recommended that a number of clarifying changes be made to the specification. The drawings were objected to under 37 CRF § 1.83(a). The final Official Action objected to claims 1, 6, 7, 8, and 11 on the grounds of insufficient antecedent basis and informalities. The final Official Action rejected claim 6 under 35 U.S.C. § 102 based on Lee et al., U.S. Patent No. 4,763,242. Claims 1, 3-5, and 7-13 were indicated to be allowable if each objection was addressed or specifically traversed and overcome. The specific recommendations, informalities and objections are addressed below.

Claim 6 has been cancelled without prejudice. Although, Applicants do not acquiesce in the art rejection of canceled claim 6, this rejection is now moot. Claims 7, 8, and 11 have been amended to be more clear and distinct. Specifically, the objection to claim 1 is traversed as discussed in the telephone interview summary below. Claim 7 has been amended to correct the antecedent basis objection by replacing the text "the first or second register files" with the text "the SP or PE register files". Claims 8 and 11 have been amended according to the suggestion in the final Official Action by replacing the term "persists" with the term "persisting". Claim 11 has also been amended according to the Examiner's suggestion by replacing "a SP register file, each PE having a register file" with the text "an SP register file and each PE having a PE register file". Claim 11 has also been amended to replace the term "the array processing" with the term "the array processor" to correct the antecedent basis objection. Claim 11 has also been amended to

address the antecedent basis objection by replacing the term "the context" with the term "the context of operation". Claim 13 has been amended to correct its status as an original claim.

Claims 1, 3-5, and 7-13 are presently pending.

Telephone Interview Summary

The Examiner is thanked for the courtesy of a telephone interview conducted on October 5, 2004. Dr. Pechanek, a co-inventor, participated with Mr. Agusta in this call. In the telephone call, the specification, Fig. 1 of the drawings, and claim 1 were discussed. Consistent with the language of claim 1, it was agreed that Fig. 1 would be amended to include an instruction register (IR) containing an SP/PE selection bit in the instruction decode & VIM controller 107. It was discussed that additional support for this change could be found in one or more of the patents incorporated by reference in the present invention. Also, consistent with the language of claim 1, it was further agreed that a processor state register is equivalent to a control register and this clarification of the term "processor state register" would be included in the specification by amendment. The MRF containing the processor state register was discussed as having an exemplary location in the data memory interface controller 125 of Fig. 1.

The final Official Action objected to claims 1, 8, and 11 for insufficient antecedent basis for the terms "CSB value" and "SP/PE selection bit value". It was argued that a bit is generally known to have a value of 0 or 1 and that a CSB (context select bit) and an SP/PE selection bit would necessarily be antecedent to the CSB value and the SP/PE selection bit value, respectively.

It was agreed that a change regarding the antecedent basis for the CSB value and the SP/PE selection bit value would not be necessary.

In response to the Examiner's request for clarification in the Official Action, we discussed Fig. 3 and pages 11 and 12 of the specification were discussed. Specifically, the notation of 1x0, 1x1, 1x2, 2x2, and a 1x5 for the PE array, where an array of PEs can be referenced as a matrix of rows and columns was discussed. For example, a 2x2 array of PEs indicates 2 rows and 2 columns of PEs or 4 PEs. Similarly a 1x1, 1x2, and 1x5 can be referenced as a single row with the specified number of columns. Consequently, a 1x1 has 1 PE, a 1x2 has 2 PEs, and a 1x5 has 5 PEs. A 1x0 has no PEs and consists only of the sequence processor (SP). It was further noted that the 1x1, 1x2, and 1x5 organizations of PEs are shown in Figs. 1, 4, and 5A/5B, respectively. It was agreed that no change to the specification was necessary.

Specification Recommendations

The final Official Action asked that the Applicants not refer to the SP/PE bit as the S/P bit in the specification in order to increase clarity by being more consistent with the claim language. Consequently, the paragraph on page 10, beginning on line 11, has been amended to include a statement of equivalency between the S/P bit and the SP/PE bit, "as specified by the instruction's S/P-bit, also referred to as the SP/PE selection bit,".

The final Official Action asked that the Applicants not refer to the CSB as the "context switch bit" in the specification to be more consistent with the term "context select bit" used in the

claims. The paragraphs beginning on page 3, line 20, and on page 9, line 18 have been amended accordingly.

The final Official Action asks that Applicants clarify in the specification what the AxB configurations mean. The meaning of the AxB configuration of PEs was discussed in the telephone interview summarized above.

Drawing Objections

The final Official Action objected to the drawings under 37 CFR § 1.83(a) for not illustrating the instruction register containing the SP/PE bit which is claimed in claim 1, the processor state register containing the CSB which is claimed in claim 1, and that these registers are independent. Fig. 1 is hereby amended to show the instruction register (IR) as part of the instruction decode and iVLIW control unit 107 with the IR containing the S/P bit. Support for adding the instruction register to Fig. 1 can be found in the original claims, as well as, in U.S. Patent No. 6,704,857 with reference to Figs. 1 and 2. This patent has been incorporated by reference in the present specification. Fig. 1 is also amended to show the processor state register, which contains the CSB as indicated in the amended paragraph beginning on page 9, line 18. The CSB is independent of the IR being in a separate location from the IR and, as described in the specification, the CSB and S/P bit are modifiable by two different types of independent operations. The amendment to Fig. 1 was discussed in the telephone interview of October 5, 2004 and agreed to by the Examiner.

Typographical Drawing Error in Fig. 5A

In preparing the amendment, it was noticed that Fig. 5A had a typographical error. Fig. 5A has been amended so that it is consistent with the connections shown for similar elements; element 551 and elements 555 and 557 of Fig. 5B.

Conclusion

All objections and informalities set forth in the final Official Action regarding claims 1, 3-5, and 7-13 have been resolved placing claims 1, 3-5, and 7-13 in order for allowance.

Respectfully submitted,

Joseph B. Agusta
Reg. No. 52,547
Priest & Goldstein, PLLC
5015 Southpark Drive, Suite 230
Durham, NC 27713-7736
(919) 806-1600

Amendments to the Drawings:

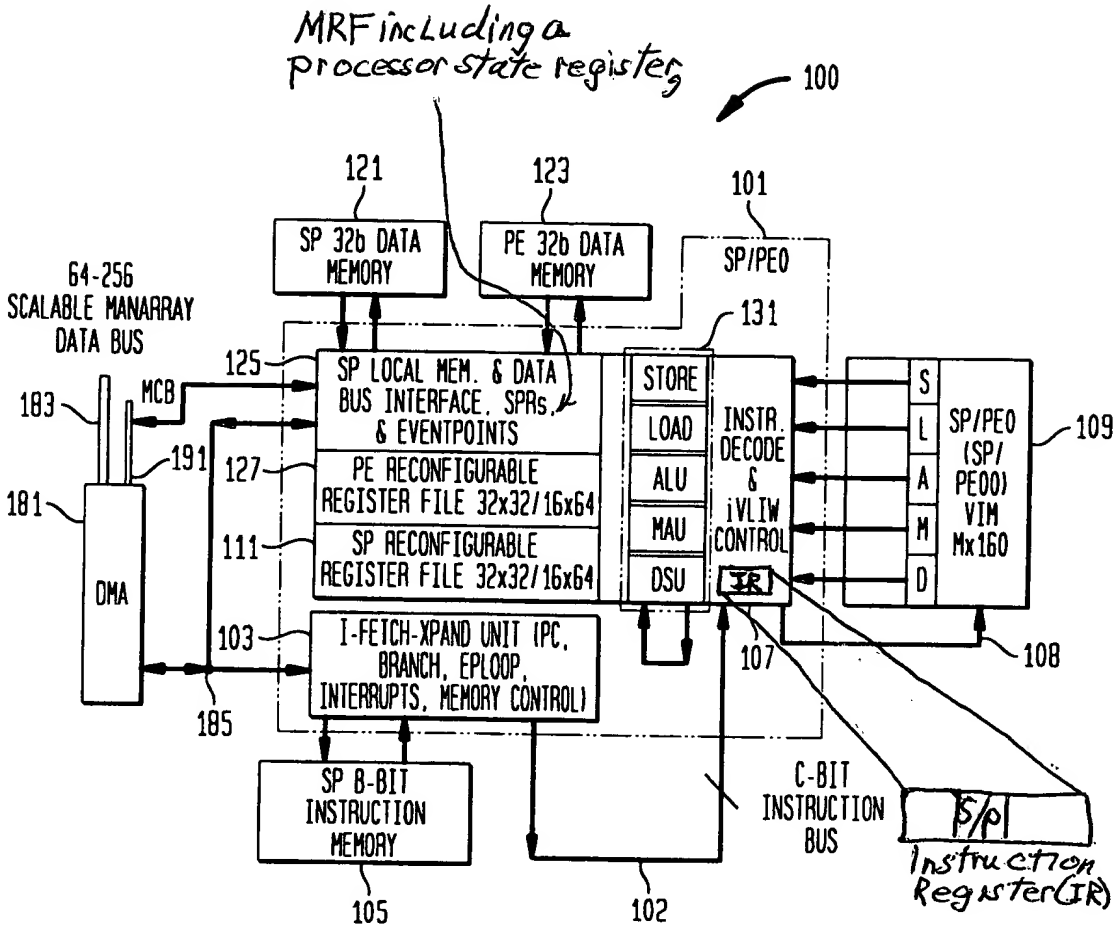
Included in the amendment are an "Annotated Sheet Showing Changes" and a "Replacement Sheet" for Figs. 1 and 5A.

Fig. 1 has been amended by agreement with the Examiner in a telephone interview summarized below. In Fig. 1, the instruction decode and iVLIW control unit 107 has been amended to show an instruction register (IR) for receiving instructions from the C-bit instruction bus 102. It is further noted that instructions stored in the IR have an S/P-bit. Also in Fig. 1, the text "MRF including a processor state register" was added to element 125 per the Examiner's requirement under 37 C.F.R. §1.83(a) that this claimed element be illustrated in the drawings.

Fig. 5A has been amended to disconnect the instruction decode and iVLIW control element found in element 553 from the Bcast data bus in order. Fig. 5A also has been amended to connect the instruction decode and iVLIW control element shown in element 553 to the C-bit instruction bus and to be consistent with the connections shown for similar elements; element 551 and elements 555 and 557 of Fig. 5B. These amendments to Fig. 5A were made to correct a typographical drawing error.

Annotated Sheet Showing Changes

FIG. 1



Annotated Sheet showing Changes



FIG. 5A